PowerMOS transistor Isolated version of PHP2N40E

PHX1N40E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a full pack, plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

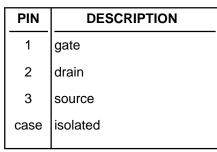
PINNING - SOT186A

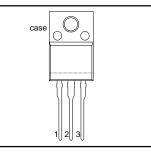
QUICK REFERENCE DATA

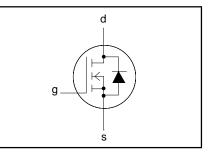
SYMBOL	PARAMETER	MAX.	UNIT
V _{DS}	Drain-source voltage	400	V
I _D	Drain current (DC)	1.75	Α
P _{tot}	Total power dissipation	25	W
R _{DS(ON)}	Drain-source on-state resistance	3.5	Ω

PIN CONFIGURATION

SYMBOL







LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DS}	Drain-source voltage		-	400	V
	Drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	400	V
V _{DGR} ±V _{GS}	Gate-source voltage		-	30	V
	Drain current (DC)	$T_{hs} = 25 \degree C$ $T_{hs} = 100 \degree C$	-	1.75	A
		$T_{hs} = 100 \text{°C}$	-	1.1	A
I _{DM}	Drain current (pulse peak value)	$T_{hs}^{hs} = 25 \text{ °C}$	-	7.0	A
I _{DR}	Source-drain diode current	$T_{hs} = 25 \degree C$	-	1.75	A
I _{DRM}	Source-drain diode current (pulse peak value)	$T_{hs} = 25 \degree C$	-	7.0	А
P _{tot}	Total power dissipation	$T_{hs} = 25 \ ^{\circ}C$	-	25	W
T _{stg}	Storage temperature		-55	150	°C
T _j	Junction temperature		-	150	°Č

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W _{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy Drain-source repetitive unclamped inductive turn-off energy	$ \begin{split} I_{D} &= 2.5 \text{ A ; } V_{DD} \leq 50 \text{ V ; } V_{GS} = 10 \text{ V ; } \\ R_{GS} &= 50 \Omega \\ T_{j} &= 25 ^{\circ}\text{C prior to surge} \\ T_{j} &= 100 ^{\circ}\text{C prior to surge} \\ I_{D} &= 2.5 \text{ A ; } V_{DD} \leq 50 \text{ V ; } \\ V_{GS} &= 10 \text{ V ; } R_{GS} &= 50 \Omega \text{ ; } T_{j} \leq 150 ^{\circ}\text{C} \end{split} $	- - -	120 20 3.6	mJ mJ mJ

1. Pulse width and frequency limited by T_{i(max)}

PHX1N40E

ISOLATION LIMITING VALUE & CHARACTERISTIC

 $T_{hs} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. \leq 65% ; clean and dustfree	-		2500	V
C _{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R _{th j-hs}	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
R _{th j-a}	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

 $T_i = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; \text{ I}_{D} = 0.25 \text{ mA}$	400	-	-	V
V _{GS(TO)}	Gate threshold voltage	$V_{DS} = V_{GS}; I_{D} = 0.25 \text{ mA}$	2.0	3.0	4.0	V
I _{DSS}	Drain-source leakage current	$V_{DS} = 400 \text{ V}; V_{CS} = 0 \text{ V}; \text{ T}_{i} = 25 \text{ °C}$	-	10	100	μA
200		$V_{DS} = 400$ V; $V_{GS} = 0$ V; $T_j = 25$ °C $V_{DS} = 320$ V; $V_{GS} = 0$ V; $T_j = 125$ °C	-	0.1	1.0	mA
I _{GSS}	Gate-source leakage current	$V_{GS} = \pm 30 \text{ V}; V_{DS} = 0 \text{ V}$	-	10	100	nA
R _{DS(ON)}	Drain-source on-state resistance	$V_{GS}^{o} = 10 \text{ V}; I_{D} = 1.25 \text{ A}$	-	3.1	3.5	Ω
V_{SD}	Source-drain diode forward voltage	$I_{F} = 2.5 \text{ A} ; V_{GS} = 0 \text{ V}$	-	1.4	2.0	V

PowerMOS transistor

Objective specification

PHX1N40E

DYNAMIC CHARACTERISTICS

 $T_i = 25$ °C unless otherwise specified

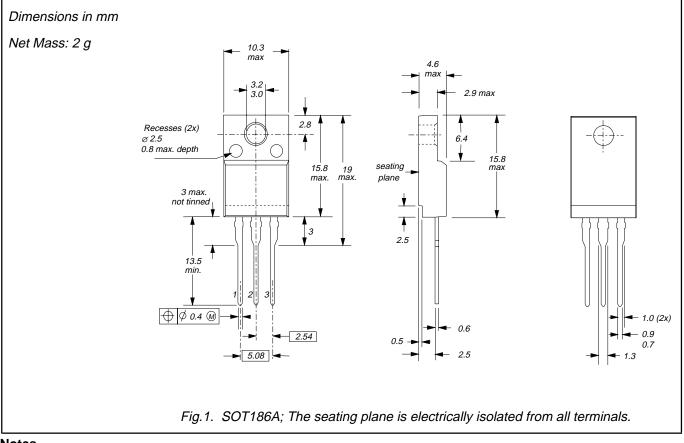
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g _{fs}	Forward transconductance	$V_{DS} = 15 \text{ V}; \text{ I}_{D} = 1.25 \text{ A}$	0.5	0.9	-	S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Feedback capacitance	$V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz$		225 30 6.0	315 42 12	ЪЪЪ
$\begin{matrix} Q_{g(tot)} \\ Q_{gs} \\ Q_{gd} \end{matrix}$	Total gate charge Gate to source charge Gate to drain (Miller) charge	V_{GS} = 10 V; I _D = 2.5 A; V _{DS} = 320 V		12 2 6	- -	nC nC nC
t _{d on} t _r t _{d off} t _f	Turn-on delay time Turn-on rise time Turn-off delay time Turn-off fall time			10 30 30 20	15 45 40 30	ns ns ns ns
t _{rr} Q _{rr}	Source-drain diode reverse recovery time Source-drain diode reverse recovery charge	$I_{F} = 2.5 \text{ A}; -dI_{F}/dt = 100 \text{ A}/\mu\text{s};$ $V_{GS} = 0 \text{ V}; \text{ V}_{R} = 100 \text{ V}$	-	350 2.5	-	ns μC
L _d L _s	Internal drain inductance Internal source inductance	Measured from drain lead 6 mm from package to centre of die Measured from source lead 6 mm from package to source bond pad	-	4.5 7.5	-	nH nH

PowerMOS transistor

Objective specification

PHX1N40E

MECHANICAL DATA



Notes

- Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
 Refer to mounting instructions for F-pack envelopes.
 Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

Data sheet status					
Objective specification This data sheet contains target or goal specifications for product development.					
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.				
Product specification	This data sheet contains final product specifications.				
Limiting values					
or more of the limiting val operation of the device at	Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.				
Application information					
Where application information is given, it is advisory and does not form part of the specification.					
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